	L #	Hits	Search Text	DBs	Time Stamp
1	L1	1507	(257/777).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/06 13:02
2	L2	953	via and L1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/06 13:02
3	L3	195	(multi-layer or multilayer) and L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/06 13:02

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	3198	(257/758).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/06 13:02
5	L5	1936	via and L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/06 13:02
6	L6	5	(second adj die or second adj chip) and (stack or stacked) and L5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/06 13:02

	L #	Hits	Search Text	DBs	Time Stamp
7	L7	20	(("5608265") or ("5874770") or ("5872025") or ("5757072") or ("6137163") or ("5128831") or ("6469374") or ("6239496") or ("5324687") or ("6849945")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/06 13:02

DOCUMENT-IDENTIFIER: US 20050014311 A1

TITLE: Multichip semiconductor device, chip therefor and
method of formation thereof

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Current US Classification, US Secondary Class/Subclass - CCSR (1):
257/777

Continuity Related Application Date - RLFD (2):
19990820

Continuity Related Application Date - RLFD (3):
19990820

Continuity Related Application Date - RLFD (4):
19971201

Summary of Invention Paragraph - BSTX (86):
[0085] wherein the vertically adjacent two chips are electrically connected
via the connecting substrate, a through-hole is formed in at least one of the
semiconductor substrates, and a conductive plug is formed in the through-hole
and connected to the connecting substrate.

Summary of Invention Paragraph - BSTX (102):
[0101] each of the vertically adjacent two chips is electrically connected
to the conductive plug **via** bumps, and

Summary of Invention Paragraph - BSTX (108):
[0107] the vertically adjacent two chips are electrically connected to each
other **via** the conductive plug, and

Brief Description of Drawings Paragraph - DRTX (10):
[0131] FIG. 8 is a sectional view of a **multilayer** interconnection in a
region where a through hole is formed;

Brief Description of Drawings Paragraph - DRTX (11):

multilayer wiring substrates 152.sub.1 and 152.sub.2. Accordingly, inexpensive, uniform **multilayer** substrates 152.sub.1 and 152.sub.2 can be formed by mass production.

Detail Description Paragraph - DETX (248):

[0389] The design rules for the wiring layers, which constitute the **multilayer** wiring substrates 152.sub.1 and 152.sub.2, are much more relaxed than those for the wiring layers which constitute the Si chips 151.sub.1 and 151.sub.2 (e.g. on the order of several .mu.m). Accordingly, a yield of nearly 100% can be achieved. Moreover, since there is no need to form devices such as MOS transistors or capacitors, there is no need to consider contamination on Si substrates, and the manufacturing process can be simplified.

Detail Description Paragraph - DETX (249):

[0390] In the present embodiment, it is assumed that the material of the chips is the same as that of the **multilayer** wiring substrates. However, these materials may differ if their thermal expansivities are nearly equal. In this case, it is preferable to use such a combination of materials that the radiation properties of the **multilayer** wiring substrate (connecting substrate) become higher than those of the chip.

Detail Description Paragraph - DETX (250):

[0391] Besides, where the same material is used, it is preferable to form the through-plugs of a material having higher radiation properties than the material of, e.g. the **multilayer** wiring substrate, by providing the **multilayer** wiring substrate with radiation means such as a radiation fin or by providing the through-plugs in the **multilayer** wiring substrate with radiation functions. Specifically, it is understood from a table of FIG. 35 that SiC or AIN can be used if the material of the chips and **multilayer** wiring substrates is Si.

connected to the
lower-layer Si chips 151.sub.2 and 151.sub.3 **via the multilayer** wiring
substrates 152.sub.1 and 152.sub.2.

Detail Description Paragraph - DETX (224):
[0365] The **multilayer** wiring substrate 152.sub.1 is connected to the
multilayer wiring substrate 152.sub.2 **via** the pads 156, solder bumps 157 and
pads 158. Similarly, the **multilayer** wiring substrate 152.sub.2 is connected to
a plastic substrate 165 **via** pads 162, solder bumps 163 and pads 164. The
plastic substrate 165 is provided with pads 166 and solder bumps 167. Wiring
layers 168 for connecting the pads 164 and 166 are formed within the plastic
substrate 165.

Detail Description Paragraph - DETX (225):
[0366] An adhesive 169 including no filler is filled between the Si chip
151.sub.1 and wiring substrate 152.sub.1 and between the Si chips 151.sub.2 and
151.sub.3 and **multilayer** wiring substrate 152.sub.2.

Detail Description Paragraph - DETX (226):
[0367] Even if the adhesive 169 includes no filler, the Si chips 151.sub.1
to 151.sub.3 and the **multilayer** wiring substrates 152.sub.1 and 152.sub.2 are
formed of the same Si. Accordingly, the thermal expansivity of the Si chips
151.sub.1 to 151.sub.3 is equal to that of the **multilayer** wiring substrates
152.sub.1 and 152.sub.2. Therefore, highly reliable connection is achieved.

Detail Description Paragraph - DETX (227):
[0368] On the other hand, since the **multilayer** wiring substrate 152.sub.2
and plastic substrate 165 are formed of different materials, an adhesive 170
including a filler is filled between the wiring substrate 152.sub.2 and plastic
substrate 165, thereby ensuring reliable connection therebetween.

Detail Description Paragraph - DETX (228):
[0369] Since no devices are formed on the **multilayer** wiring

substrates
152.sub.1 and 152.sub.2, the pitch of solder bumps 163 can be set at a desired
value. The pitch of solder bumps 163 may be set at such a value that the
adhesive 170 can be surely put among the solder bumps 163.

Detail Description Paragraph - DETX (229):
[0370] As has been described above, in the present embodiment, since the
multilayer wiring substrates 152.sub.1 and 152.sub.2 and Si chips 151.sub.1 to
151.sub.3 are formed of the same Si, thermal strain hardly occurs in the solder
bumps 154 and 160.

Detail Description Paragraph - DETX (230):
[0371] Accordingly, even if the integration density of the Si chips
151.sub.1 to 151.sub.3 further increases and the distance between the Si chip
151.sub.1 and **multilayer** wiring substrate 152.sub.1, as well as between the Si
chips 151.sub.2 and 151.sub.3 and **multilayer** wiring substrate 152.sub.2,
further decreases, the reliable connection therebetween is ensured.
Accordingly, reliable connection between the upper-layer Si chip 151.sub.1 and
the lower-layer Si chips 151.sub.2 and 151.sub.3 is ensured.

Detail Description Paragraph - DETX (231):
[0372] Since the **multilayer** wiring substrates 152.sub.1 and 152.sub.2 and Si
chips 151.sub.1 to 151.sub.3 are formed of the same Si, there is no need to
make their thermal strains close to each other, and the adhesive 169 including
no filler can be used.

Detail Description Paragraph - DETX (232):
[0373] Accordingly, even if the integration density of the Si chips
151.sub.1 to 151.sub.3 further increases and the distance between the Si chip
151.sub.1 and **multilayer** wiring substrate 152.sub.1, as well as between the Si
chips 151.sub.2 and 151.sub.3 and **multilayer** wiring substrate 152.sub.2,
further decreases, there occurs no region which is not filled with the adhesive

169. Therefore, reliable connection between the upper-layer Si chip 151.sub.1
and the lower-layer Si chips 151.sub.2 and 151.sub.3 is ensured.

Detail Description Paragraph - DETX (234):
[0375] In the present embodiment, since there is no need to form through-plugs in the Si chips 151.sub.1 to 151.sub.3 on which devices are
formed, a rise in manufacturing cost can be suppressed. Needless to say, it is
possible to connect the Si chip 151.sub.1 to the Si chips 151.sub.2 and
151.sub.3 **via** the multichip wiring substrate 152.sub.1 by using the Si chips Si
chips 151.sub.1 to 151.sub.3 having through-plugs.

Detail Description Paragraph - DETX (237):
[0378] As is shown in FIG. 34B, the through-plugs 104 of Si, wiring layer
and pads 155 are formed on the Si substrate, thus constituting the **multilayer**
wiring substrate 152.sub.1. The pads 155 are formed at positions corresponding
to the pads 153. Each of pads 153 and 155 has a square shape with each of 20
.mu.m. The pitch of the pads 153 and 155 is set at 30 .mu.m (the distance
between adjacent pads is 10 .mu.m).

Detail Description Paragraph - DETX (238):
[0379] In a step shown in FIG. 34C, the solder bumps 154 of Si chip
151.sub.1 are aligned with the pads 155 of **multilayer** wiring substrate
152.sub.1, and these are bonded to each other. The epoxy adhesive 169
including no filler is filled between the Si chip 151.sub.1 and **multilayer**
wiring substrate 152.sub.1. Thus, a unit 171.sub.1 wherein the Si chip
151.sub.1 is bonded by flip-chip bonding to the **multilayer** wiring substrate
152.sub.1 is formed.

Detail Description Paragraph - DETX (239):
[0380] The distance between the Si substrate constituting the **multilayer**
wiring substrate 152.sub.1 and the Si substrate constituting the Si chip
151.sub.1 is set at 20 .mu.m. Accordingly, the size of each solder

bump 154 is
set at about 20 .mu.m.phi..

Detail Description Paragraph - DETX (241):
[0382] As is shown in FIG. 34E, the through-plugs 104 of Si, wiring layer
and pads 158, 159 and 162 are formed on the Si substrate, thus constituting the
multilayer wiring substrate 152.sub.2. The solder bumps 157 are formed on the
pads 158.

Detail Description Paragraph - DETX (242):
[0383] As is shown in FIG. 34F, like the unit 1711, alignment, bonding and
filling of adhesive 169 are carried out, and a unit 171.sub.2 wherein the Si
chip 151.sub.2 and Si chip 151.sub.3 are bonded by flip-chip bonding to the
multilayer wiring substrate 152.sub.2 is formed.

Detail Description Paragraph - DETX (244):
[0385] Since the **multilayer** wiring substrates 152.sub.1 and 152.sub.2 and Si
chips 151.sub.2 and 151.sub.3 are formed of Si, no thermal strain occurs due to
a difference in thermal expansivity. Accordingly, the size and pitch of bumps
may be determined by considering only the thickness of the Si chip 151.sub.2,
151.sub.3 between the **multilayer** wiring substrates 152.sub.1 and 152.sub.2,
without considering thermal strain due to a difference in thermal expansivity.

Detail Description Paragraph - DETX (245):
[0386] Since the pads 162 formed on the lower surface of the **multilayer**
wiring substrate 152.sub.2 are to be connected to the solder bumps 163 of
plastic substrate 165, it is necessary that the diameter of each pad 162 and
the pitch of pads 162 be set at about 100 .mu.m or more and at about 200 .mu.m
or more, respectively. A wiring layer for relaxing the pitch is formed on the
multilayer wiring substrate 152.sub.2.

Detail Description Paragraph - DETX (247):
[0388] In the present embodiment, Si substrates are used for the